Indian Institute of Technology Patna

Dept. of Electrical Engineering

Bihta, Patna, Bihar – 801106

**Name -** Madan Kumar Jha

**Roll No. –** 2411EE23

**Project** – Classical PLL

**Date** – 13/06/2025

**Designing a Complete PLL**

**Theory:**

**Type-II, 3rd Order Phase-Locked Loop (PLL) Design**

A Phase-Locked Loop (PLL) synchronizes the phase and frequency of a generated signal with a reference signal. A Type-II, 3rd order PLL consists of a Phase Frequency Detector (PFD), Charge Pump, Loop Filter, Voltage-Controlled Oscillator (VCO), and a Frequency Divider. The PFD, designed using a NOR latch, compares the phase and frequency of the input and feedback signals, generating UP and DOWN signals. The charge pump then converts these signals into an analog current, which is further smoothed by the loop filter consisting of R1, C1, and C2. This control voltage drives a current-starved VCO, generating a corresponding output frequency. The output is divided by a factor of 48 using a divider circuit, and the feedback is compared with the reference to achieve phase lock.

The Type-II, 3rd order PLL is preferred for its improved noise performance and stability. By using a third-order loop filter, the system effectively suppresses high-frequency noise. Careful design considerations, such as optimizing the loop filter components and ensuring proper biasing of the VCO, contribute to minimizing phase noise. Additionally, selecting an appropriate charge pump current and divider ratio ensures faster lock time and reliable frequency synthesis. This design is widely used in applications like clock generation, frequency synthesis, and communication systems.

**Circuit Diagrams:**

A complete type -II 3rd order PLL is shown below

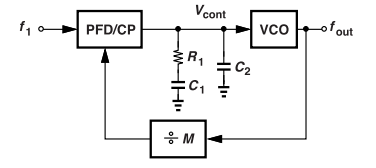


Fig.1: A complete PLL

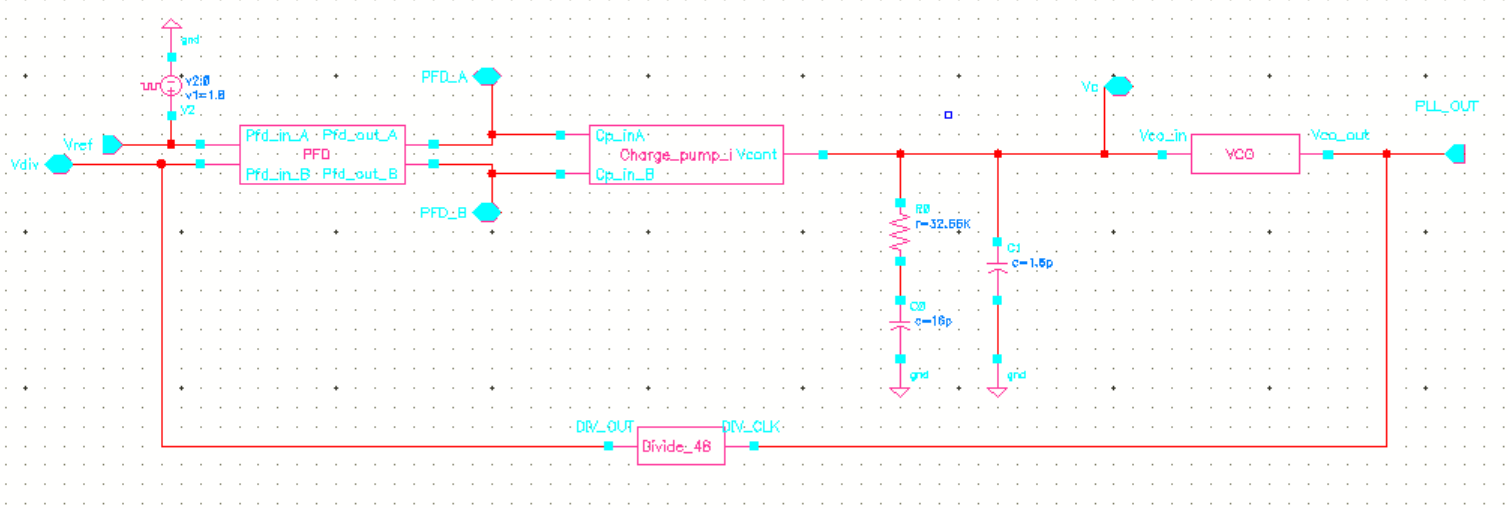


Fig 2: PLL Schematic on Cadence

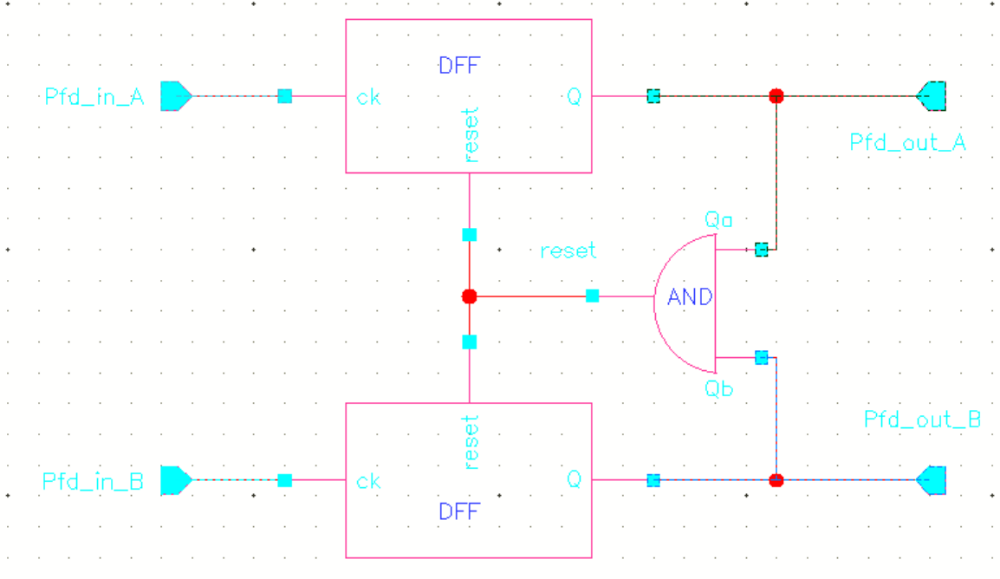
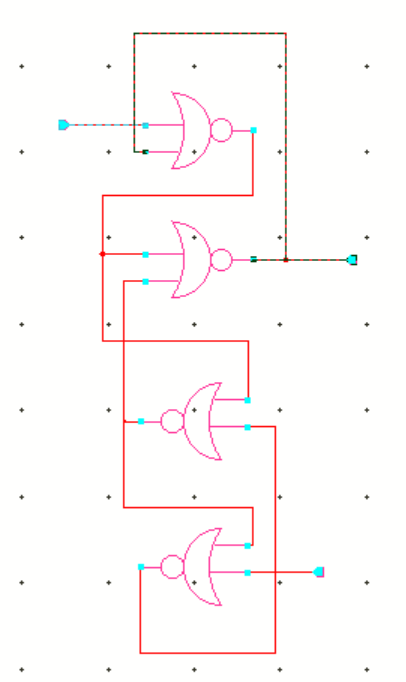
 

Fig 3 (a) : PFD Schematic on Cadence Fig (b) :Schematic of DFF used in PFD

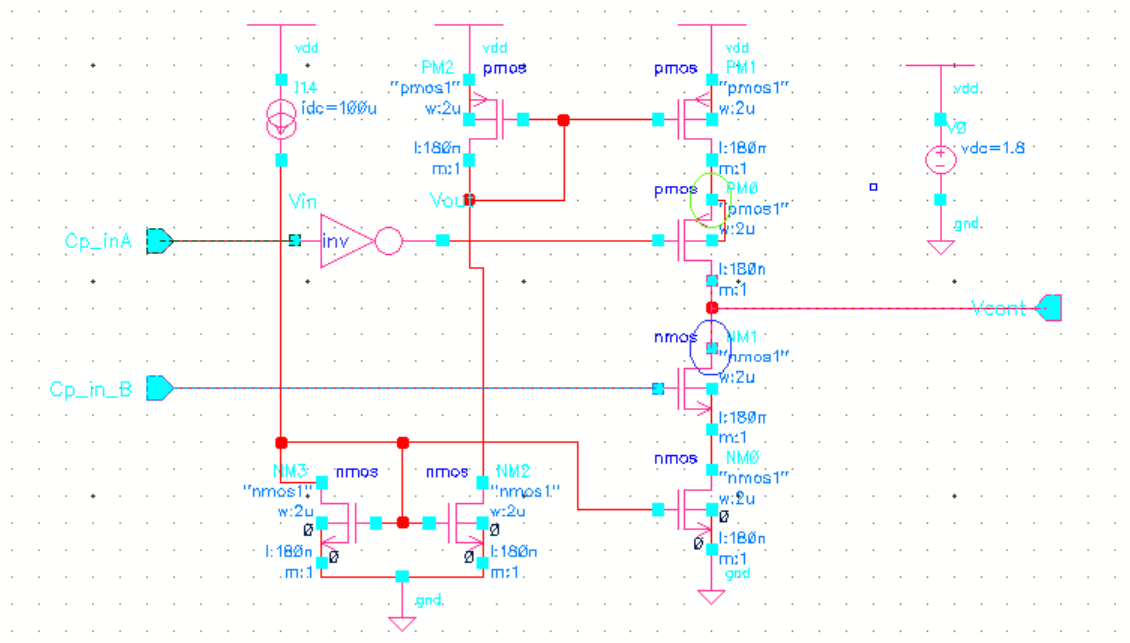


Fig 4: Charge pump Schematic on Cadence

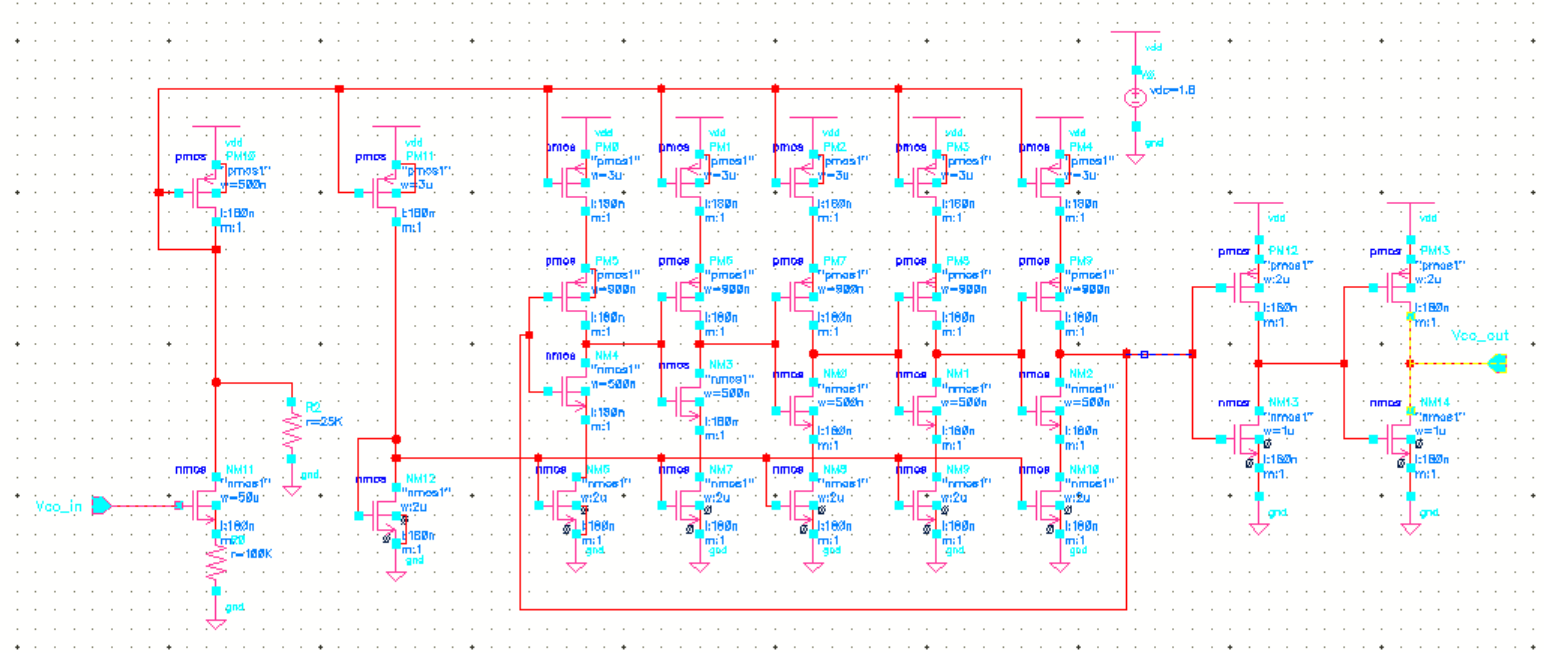


Fig 5: VCO Schematic on Cadence

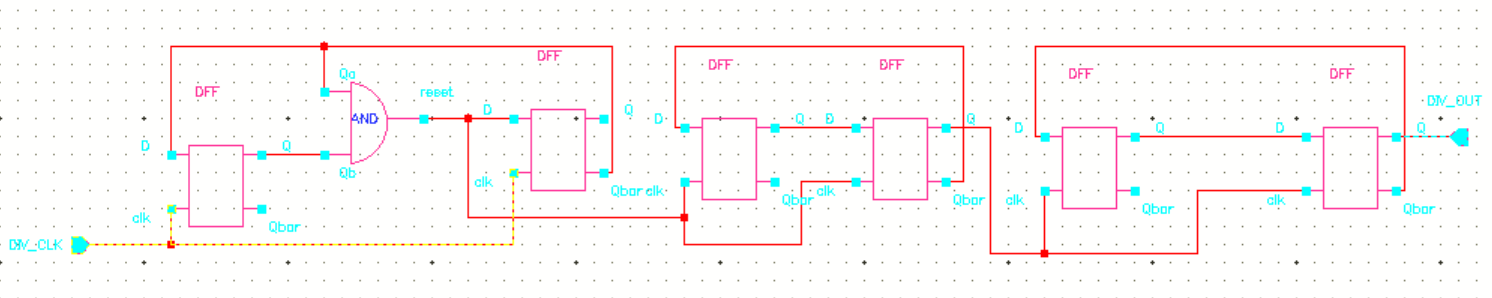


Fig 6 (a): Divider Schematic on Cadence

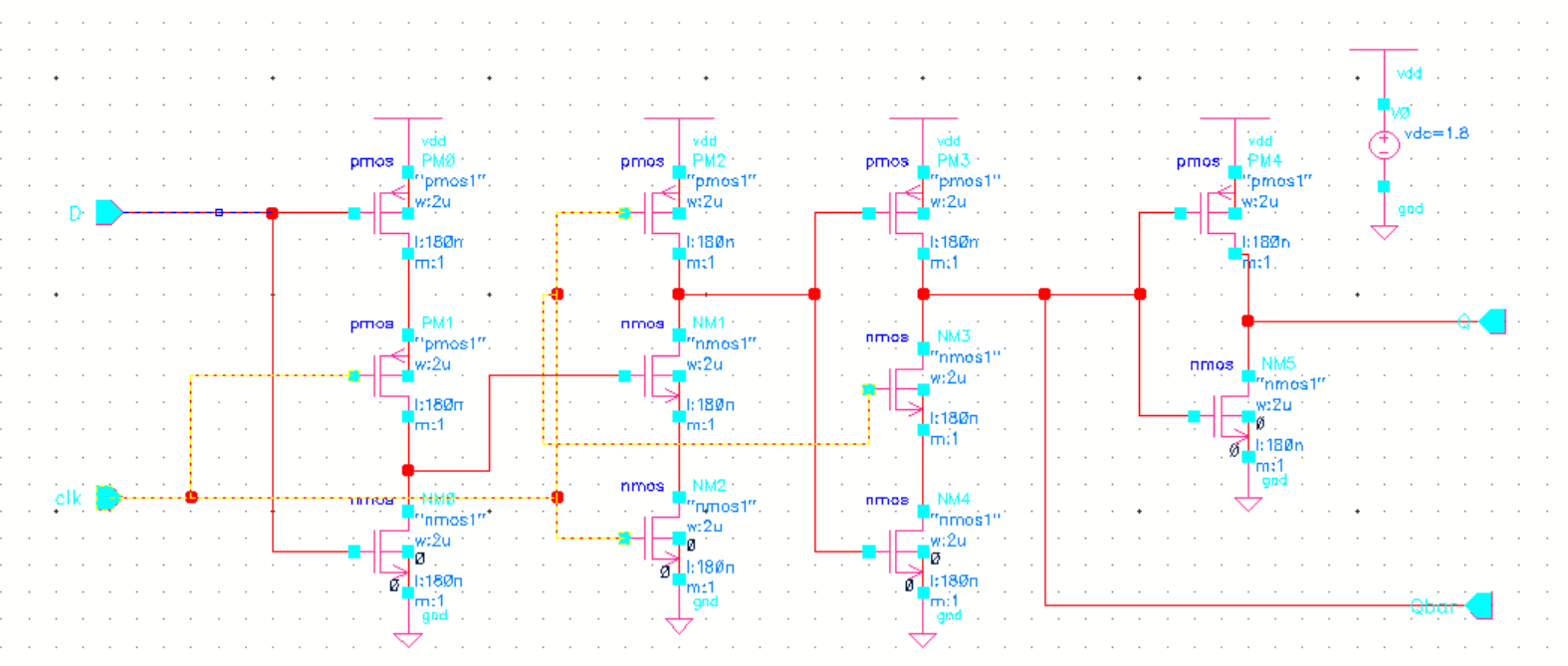
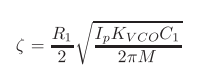


Fig 6 (b): DFF used in divider

**Design the PLL** : Finding R1, C1, C2, N to get fo=1.942 GHz

**Given:** (i) Reference frequency, fref= 40.46 MHz, (ii) fo=1.942GHz (iii) ζ=1

**Use** Charge pump current Ip = 100 uA, VCO Gain, KVCO = 112.5 MHz ( Experimently get from VCO experiment )

, , 

C2= 0.1 C1.

**Result**

From calculation, I get

C1 = 16 pF

C2 = 1.6 Pf,

R1 = 32.66 Kohm,

Kvco = 112.5 MHz /V

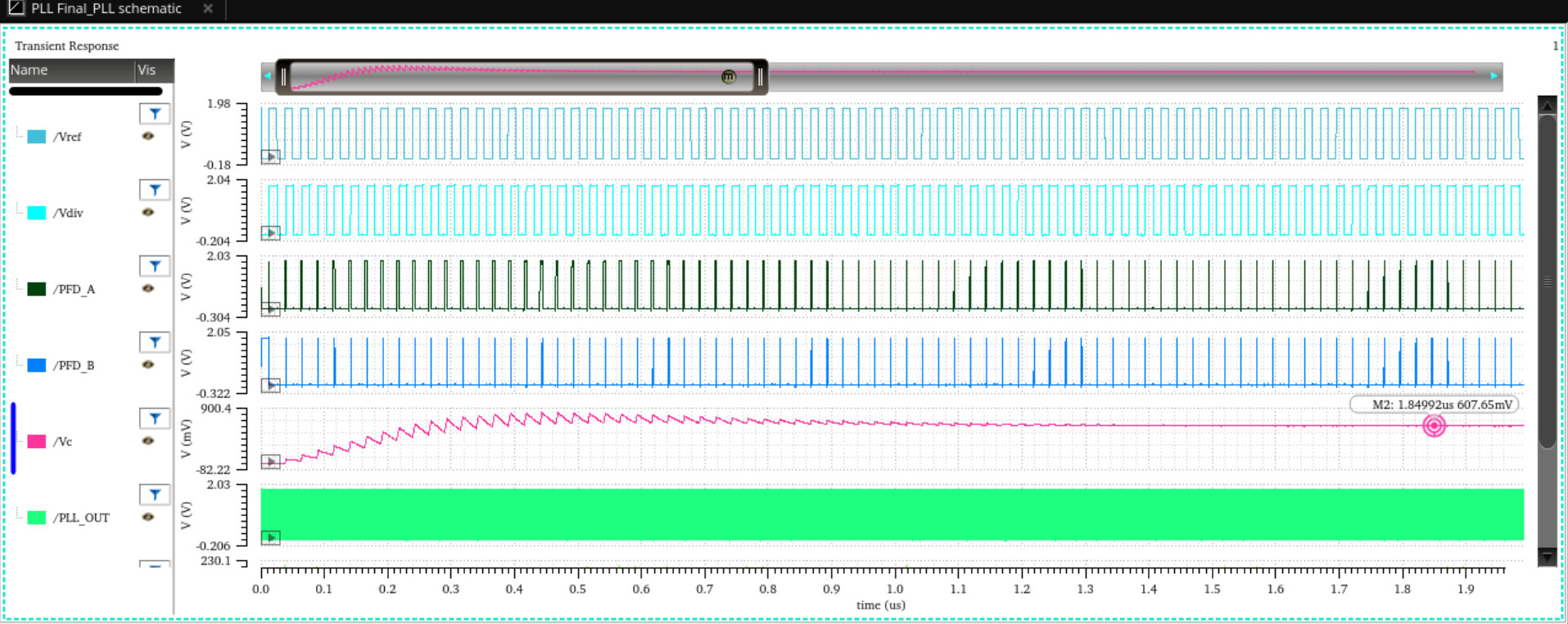


Fig 7: Output Plot for various parameter of PLL

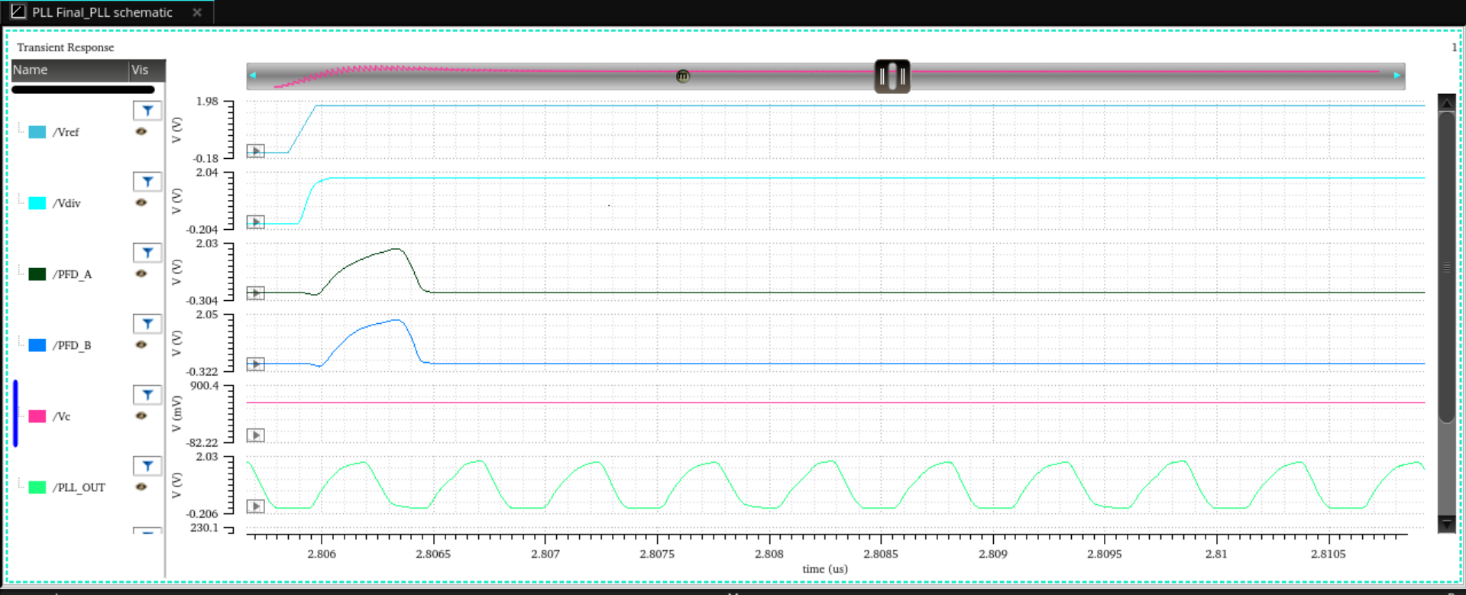


Fig 8: Output waveform of output of VCO

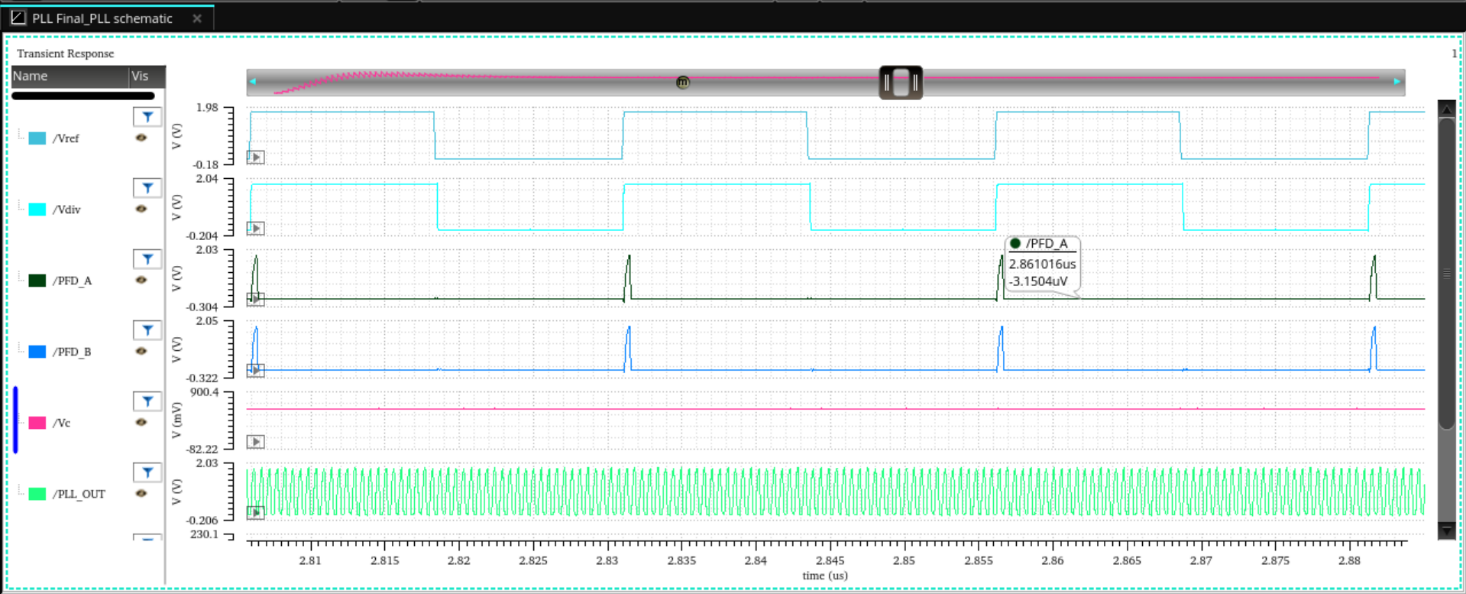


Fig 9: Output waveform of PFD

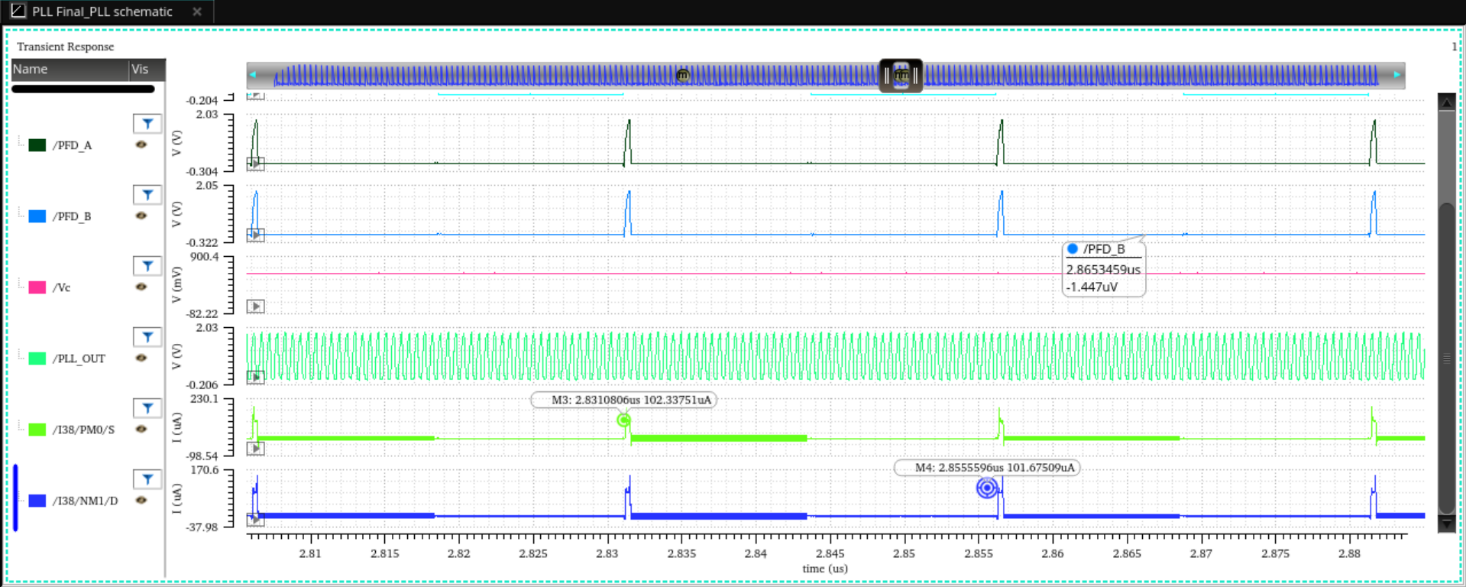


Fig 10: Output waveform of charge pump current.

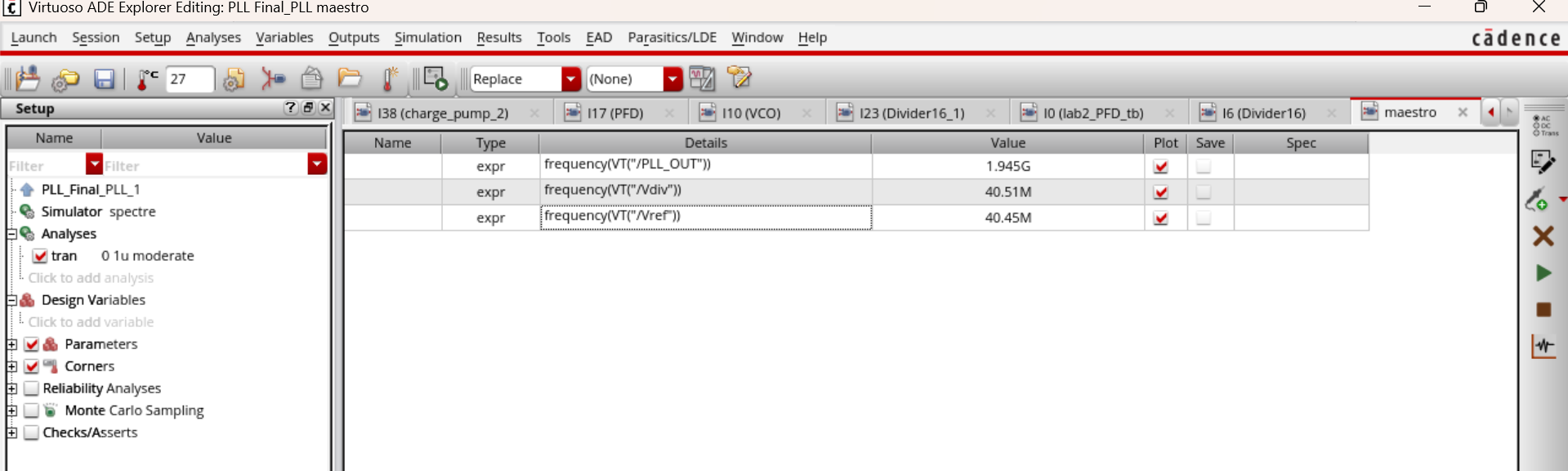


Fig 11: Output frequency of PLL, Reference frequency and Feedback frequency of divider.

***LOCKING ACHIEVED SUCCESSFULLY AT 607 mV !!***